

Thyristor Surge Suppressors (TSS)

PXXX0SD Series

DO-214AA(SMB)

@10/700 μ S, 8KV

Description

PXXX0SD Series are designed to protect broadband equipment such as modems, line card, CPE and DSL from damaging over-voltage transients.

The series provides a surface mount solution that enables equipment to comply with global regulatory standards.

Features and Benefits

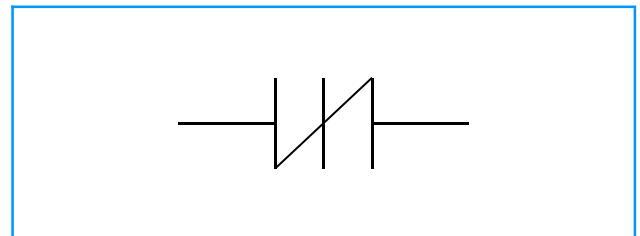
- ◆ Low voltage overshoot
- ◆ Low on-state voltage
- ◆ Does not degrade surge capability after multiple surge events within limit
- ◆ Fails short circuit when surged in excess of ratings
- ◆ Low Capacitance

Applicable Global Standards

- ◆ TIA-968-A
- ◆ ITU K.20/21 Enhanced level
- ◆ ITU K.20/21 Basic Level
- ◆ GR 1089 Inter building
- ◆ GR 1089 Inter building
- ◆ IEC 6100-4-5
- ◆ YD/T 1082
- ◆ YD/T 993
- ◆ YD/T 950



Schematic Symbol



Electrical Parameters

Parameter	Definition
I_S	Switching Current - maximum current required to switch to on state
I_{DRM}	Leakage Current - maximum peak off-state current measured at V_{DRM}
I_H	Holding Current - minimum current required to maintain on state
I_T	On-state Current - maximum rated continuous on-state current
V_S	Switching Voltage - maximum voltage prior to switching to on stat
V_{DRM}	Peak Off-state Voltage - maximum voltage that can be applied while maintaining off state
V_T	On-state Voltage - maximum voltage measured at rated on-state current
C_O	Off-state Capacitance - typical capacitance measured in off state

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Electrical Characteristics (T_A=25°C)

Part Number	Marking	V _{DRM} @I _{DRM} =1 μ A	V _S ① @100V/ μ S	I _S	V _T @I _T =2.2A	I _T	I _H	C ₀ ② @1MHz, 2V bias
		V Min.	V Max.	mA max.	V Max.	A Max.	mA Min.	pF Typ.
P0080SD	P-8D	6	15	800	4	2.2	50	150
P0640SD	P06D	58	77	800	4	2.2	50	150
P0720SD	P07D	65	87	800	4	2.2	50	150
P0900SD	P09D	75	98	800	4	2.2	50	140
P1100SD	P11D	90	130	800	4	2.2	50	110
P1300SD	P13D	120	160	800	4	2.2	50	100
P1500SD	P15D	140	180	800	4	2.2	50	90
P1800SD	P18D	170	220	800	4	2.2	50	90
P2300SD	P23D	190	260	800	4	2.2	50	80
P2600SD	P26D	220	300	800	4	2.2	50	70
P3100SD	P31D	275	350	800	4	2.2	50	60
P3500SD	P35D	320	400	800	4	2.2	50	60
P3800SD	P38D	340	450	800	4	2.2	50	60
P4200SD	P42D	400	520	800	4	2.2	100	40

Notes:

- ① V_S is measured at 100KV/s.
- ② Off-state capacitance is measured in V_{DC}=2V, V_{RMS}=1V, f=1MHz.

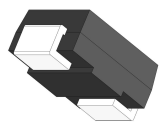
Surge Ratings

Series	2/10 μ S ¹	8/20 μ S ¹	10/160 μ S ¹	10/560 μ S ¹	10/1000 μ S ¹	5/310 μ S ¹	I _{TSM} 50/60 Hz	di/dt
	2/10 μ S ²	1.2/50 μ S ²	10/160 μ S ²	10/560 μ S ²	10/1000 μ S ²	10/700 μ S ²		
	A min	A min	A min	A min	A min	A min		
D	800	700	--	--	200	200	70	500

Notes:

- 1. Current waveform in μ s
- 2. Voltage waveform in μ s
- Peak pulse current rating (I_{PP}) is repetitive and guaranteed for the life of the product.
- I_{PP} ratings applicable over temperature range of -40°C to +85°C
- The device must initially be in thermal equilibrium with -40°C < T_J < +150°C

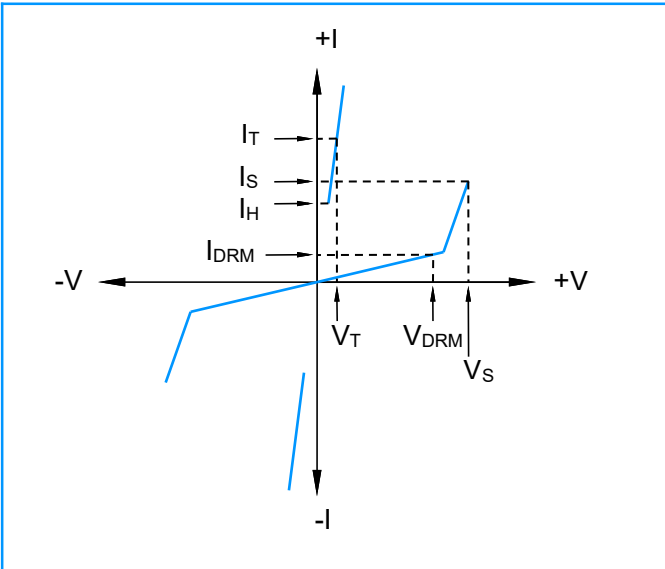
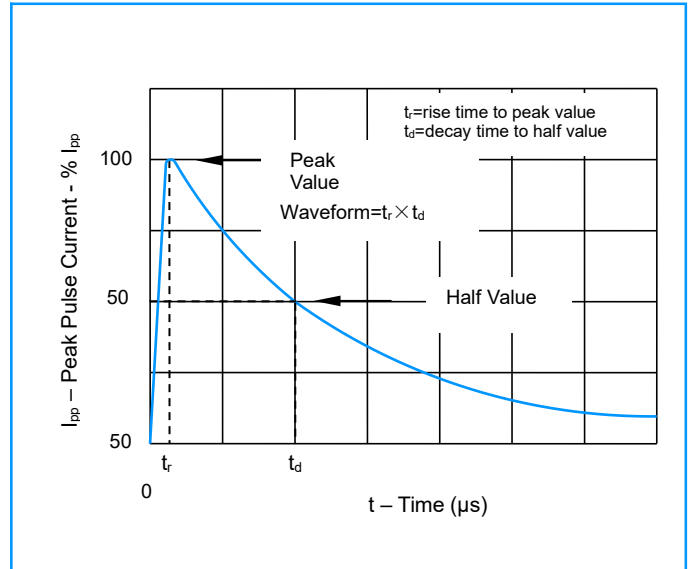
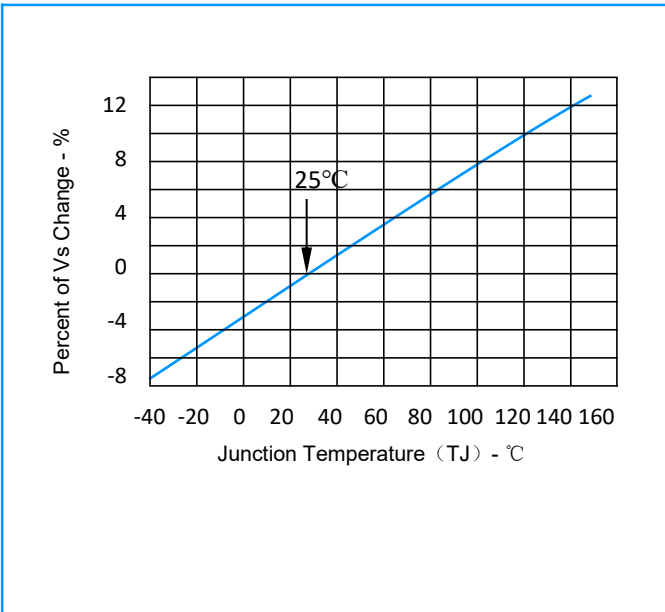
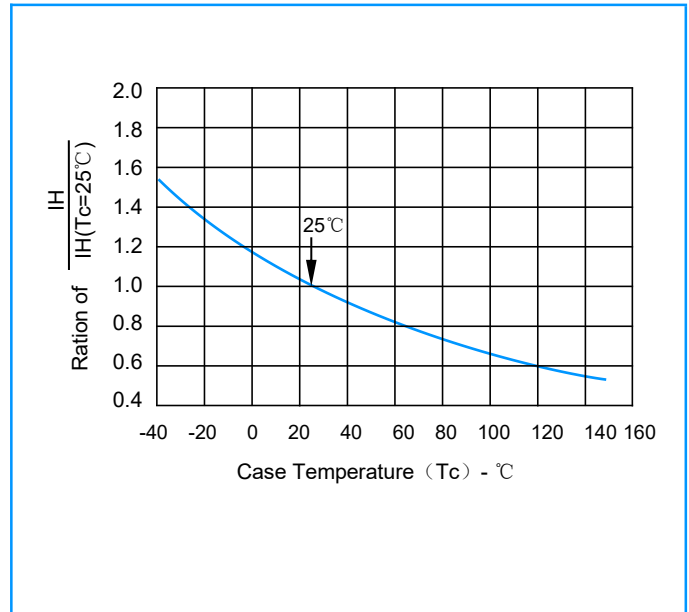
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
DO-214AA(SMB) 	T _J	Operating Junction Temperature Range	- 40 to + 125	°C
	T _S	Storage Temperature Range	- 60 to +150	°C
	R _{θJA}	Thermal Resistance: Junction to Ambient	90	°C/W

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Characteristic Curves

Figure 1 - V-I Characteristics

Figure 2. $t_r \times t_d$ Pulse Waveform

Figure 3 - Normalized V_S Change Versus Junction Temperature

Figure 4 - Normalized DC Holding Current Versus Case Temperature


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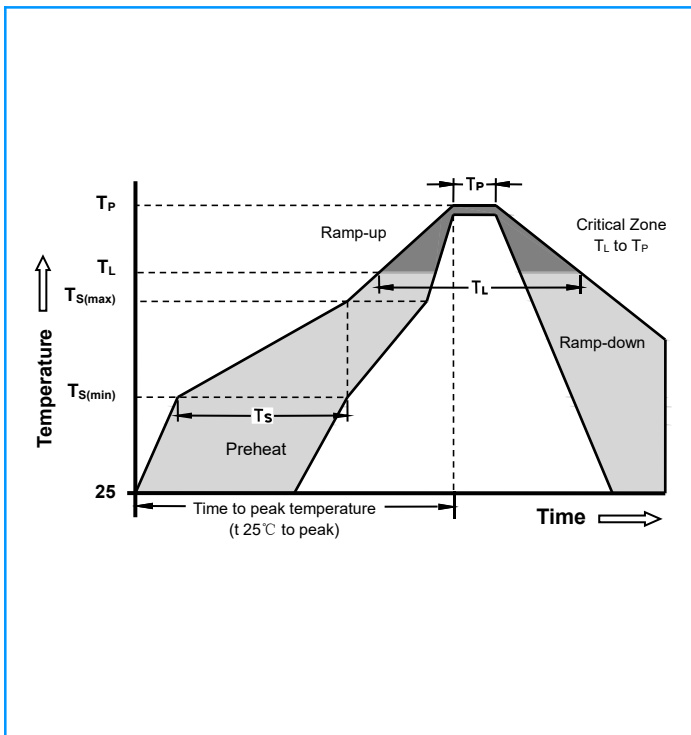
Environmental Specifications

High Temp Voltage Blocking	80% Rated VDRM (VAC Peak) +125 °C or +150 °C, Lead Material Copper Alloy High Temp Voltage Blocking 504 or 1008 hrs. MIL-STD-750 (Method 1040) JEDEC, JESD22-A-101
Temp Cycling	-65 °C to +150 °C, 15 min. dwell, 10 up to 100 cycles. MIL-STD-750 (Method 1051) EIA/JEDEC, JESD22-A104
Biased Temp & Humidity	52 VDC (+85 °C) 85%RH, 504 up to 1008 hrs. EIA/JEDEC, JESD22-A-101
High Temp Storage	+150 °C 1008 hrs. MIL-STD-750 (Method 1031) JEDEC, JESD22-A-101
Low Temp Storage	-65 °C, 1008 hrs.
Thermal Shock	0 °C to +100 °C, 5 min. dwell, 10 sec. transfer, Thermal Shock 10 cycles. MIL-STD-750 (Method 1056) JEDEC, JESD22-A-106
Autoclave (Pressure Cooker Test)	+121 °C, 100%RH, 2atm, 24 up to 168 hrs. EIA/Cooker Test) JEDEC, JESD22-A-102
Resistance to Solder Heat	+260 °C, 30 secs. MIL-STD-750 (Method 2031)
Moisture Sensitivity Level	85%RH, +85 °C, 168 hrs., 3 reflow cycles Level (+260 °C Peak). JEDEC-J-STD-020, Level 1

Physical Specifications

Lead Material	Copper Alloy
Terminal Finish	100% Matte-Tin Plated
Body Material	UL recognized epoxy meeting flammability classification 94V-0

Soldering Parameters

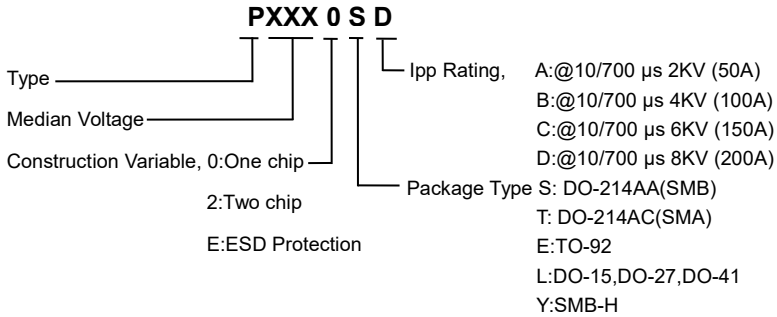


Reflow Condition		Lead-free assembly
Pre Heat	-Temperature Min ($T_{S(min)}$)	+150 °C
	-Temperature Max ($T_{S(max)}$)	+200 °C
	-Time (min to max) (T_S)	60 -180 Seconds
Average ramp up rate (Liquidus Temp T_L to peak)		3 °C/Second Max
$T_{S(max)}$ to T_L - Ramp-up Rate		3 °C/Second Max
Reflow	- Temperature (T_L) (Liquidus)	+217 °C
	- Time (min to max) (T_L)	60 -150 Seconds
Peak Temperature (T_P)		260 (+0/-5) °C
Time within 5 °C of actual peak Temperature (t_p)		30 Seconds Max
Ramp-down Rate		6 °C/Second Max
Time 25 °C to peak Temperature (T_P)		8 minutes Max
Do not exceed		+260 °C

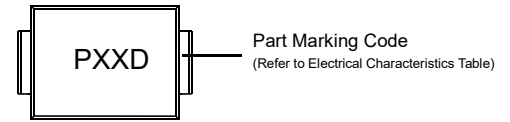
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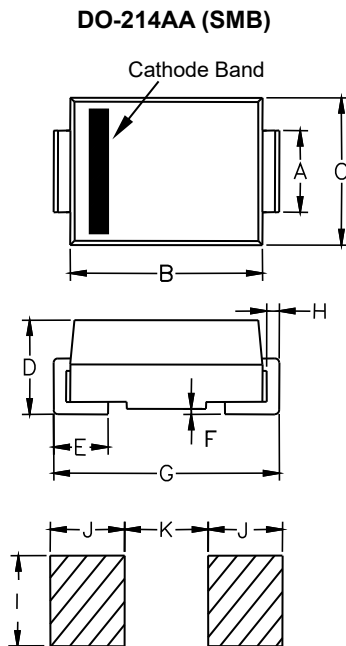
Part Numbering



Part Marking



Dimensions



Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	0.075	0.087	1.90	2.20
B	0.169	0.189	4.30	4.80
C	0.130	0.155	3.30	3.94
D	0.083	0.094	2.10	2.40
E	0.037	0.060	0.95	1.52
F	0.002	0.008	0.051	0.203
G	0.205	0.220	5.20	5.60
H	0.006	0.012	0.15	0.31
I	0.091	-	2.23	-
J	0.087	-	2.20	-
K	-	0.102	-	2.60

Packaging

Part Number	Component Package	Quantity	Packaging Option	Packaging Specification
Pxxx0SD	DO-214AA(SMB)	3000 PCS	Tape & Reel -12mm/13"tape	EIA -481 - D

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Tape and Reel Specifications

